IASET: International Journal of Electronics
and Communication Engineering (IJECE)
ISSN (P): 2278-9901; ISSN (E): 2278-991X
Vol. 5, Issue 4, Jun – Jul 2016; 23-28

International Academy of Science,
Engineering and Technology
Connecting Researchers; Nurturing Innovations

IMPLEMENTATION OF ADVANCED UART CONTROLLER

JYOTI APPASHEB LOKHANDE

PG Scholar, E & TC Department, G. H. Raisoni College of Engineering & Management,

Chas, Ahmednagar, Maharashtra, India

ABSTRACT

This paper presents advanced UART controller with configurable baud rate. UART a kind of serial communication circuit is used widely. In parallel communication the cost as well as complexity of the system increases due to simultaneous transmission of data bits on multiple wires. Serial communication alleviates this drawback of parallel communication and emerges effectively in many applications for long distance communication as it reduces the signal distortion because of its simple structure. Architecture of UART implemented on the Spartan 6 Series FPGA using Verilog description language based on FIFO technique to achieve reliable serial data communication. An Asynchronous FIFO is designed with read and writes pointers. The design of Controller is used to implement communication when transmitter Device and receiver Device are set at different Baud rates. The baud rates are synchronized using switches at the input side of FPGA & at the Output side of FPGA. It reduces the synchronization error between subsystems in system with other subsystem. This Paper presents the structure of UART controller as scalable and reconfigurable design. This design can effectively use for communication between two devices with different baud rates. The overall design is simulated on Xilinx ISE simulator.

KEYWORDS: UART (Universal Asynchronous Receiver Transmitter), FIFO (First in First Out)